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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,733	10/08/2003	Warren A. Seith	091393-9208	6695
23585	7590 07/29/2004		EXAMINER	
MICHAEL BEST & FRIEDRICH LLP 3773 CORPORATE PARKWAY			NASRI, JAVAID H	
SUITE 360 CENTER VALLEY, PA 18034-8217			ART UNIT	PAPER NUMBER
		7	2839	

DATE MAILED: 07/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)				
	10/681,733	SEITH ET AL.				
Office Action Summary	Examiner	Art Unit				
	Javaid_Nasri	2839				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPL THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1. after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a rep If NO period for reply is specified above, the maximum statutory period Failure to reply within the set or extended period for reply will, by statut Any reply received by the Office later than three months after the mailir earned patent term adjustment. See 37 CFR 1.704(b).	136(a). In no event, however, may a reply be timely within the statutory minimum of thirty (30) days will apply and will expire SIX (6) MONTHS from e, cause the application to become ABANDONE	nely filed s will be considered timel the mailing date of this co				
Status						
1) Responsive to communication(s) filed on						
	s action is non-final.					
3)☐ Since this application is in condition for allower		secution as to the	e merits is			
closed in accordance with the practice under	•					
Disposition of Claims						
4) ⊠ Claim(s) <u>1-20</u> is/are pending in the application 4a) Of the above claim(s) is/are withdra 5) □ Claim(s) is/are allowed. 6) ⊠ Claim(s) <u>1-20</u> is/are rejected. 7) □ Claim(s) is/are objected to. 8) □ Claim(s) are subject to restriction and/or	wn from consideration.	,				
Application Papers						
9) The specification is objected to by the Examina  10) The drawing(s) filed on <u>08 October 2003</u> is/are  Applicant may not request that any objection to the  Replacement drawing sheet(s) including the correct  11) The oath or declaration is objected to by the E	e: a) accepted or b) objected if the drawing(s) is objection is required if the drawing(s) is objection is required if the drawing(s) is objection is required if the drawing(s) is objected or b).	e 37 CFR 1.85(a). jected to. See 37 CF	FR 1.121(d).			
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of:  1. Certified copies of the priority documen 2. Certified copies of the priority documen	ts have been received.		. <u> </u>			
<ol><li>Copies of the certified copies of the price</li></ol>	•	ed in this National	Stage			
application from the International Burea * See the attached detailed Office action for a list	, , , ,	.d				
Attachment(s)  1) Notice of References Cited (PTO-892)	4)  Interview Summary					
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Da	ate	O 152)			
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08 Paper No(s)/Mail Date 10/8/03.	) 5) Notice of Informal P 6) Other:	atent Application (PTC	J-10Z)			

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## **DETAILED ACTION**

# Specification

- 1. The disclosure is objected to because of the following informalities:
  - a) On page 5, line 4, change "and" to -- end --.

Note: These are few examples only. Applicant is required to check the entire disclosure and correct the disclosure accordingly.

## Claim Objections

- 2. Claims 14 and 17-20 are objected to because of the following informalities:
  - a) In claim 14, line 1, "the main board" lacks antecedent base.
  - b) In claim 17, a) one hole is not configured to receive a plurality of connector pins. One hole is configured to receive only one pin. b) There is only one slot for receiving a main circuit board not slots.
  - c) In claim 20, line 2, "the bonding rings" lacks antecedent base.

Appropriate correction is required.

Note: These are few examples only. Applicant is required to check all the claims and correct them accordingly.

#### Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 4. Claims 13-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Malhi et al (4,922,378, cited in IDS).

Malhi et al discloses for claim 13, a main circuit board (10) having a first face and a second face and terminating in an edge having a mounting area (see figures 1-3), the mounting area configured for receiving a connector board (12) and comprising at least one mounting pad (16, 18) on at least one of the first and the second faces, for claim 14, the edge of the main board adjacent the mounting area includes a slot (14, see figure 2) with adjacent tab portions (30, 28) for receiving a connector board, the at least one mounting pad (16) is a plurality of electrical contact pads located on one of the first side of the connector board (see figure 1), for claim 16, the printed circuit board comprises traces connecting at least one of the electrical contact pads to at least one electrical component located on the printed circuit board.

5. Claims 1, 3, 4, 6-9, 11, 12, 17, 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Hanni et al (4,109,298, cited in IDS).

Hanni et al discloses for claim 17, a first face and a second face and a thickness having slot (51, see figure 2) for receiving a main printed circuit board (1) and at least one through hole (5) between the first and second faces configured to receive a plurality of connector pin (4), for claim 19, the each of the plurality of holes located in the connector board comprises bonding rings plated (6) around their periphery on one side of the corrector board, for claims 11 and 20, the connector board is a printed circuit board with traces that electrically connect the bonding rings, For claim 1, a main board (1, 2) having a first face and a second face and terminating in

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an edge having a mounting area, the mounting area comprising at least one mounting pad on at least one of the first and the second faces; a connector board (1, 2) having a first face and a second face and comprising at least one through hole (5) between the first and second faces; and at least one connector pin (4) disposed in the at least one through hole and having a portion extending beyond each of the first and second faces of the connector board (see figure 3), wherein the edge of the main board and the second face of the connector board are abutted and the portion of the connector pin extending beyond the second face of the connector board is attached to the at least one mounting pad (note: pads are claimed very broadly, 6 can be read as pads and tip of 4 can be read as pads), for claim 3, the at least one mounting pad is a plurality of electrical contact pads located on the first side of the connector board, for claim 4, the at least one hole in the connector board is a plurality of holes and the at least one pin is a plurality of corresponding connector pins inserted in the plurality of holes, for claim 6, the plurality of connector pins include at least one row of pins aligned with and attached to the plurality of electrical contact pads on edge of the main board, for claim 7, the portion of at least one row of pins extending beyond the second face of the connector board are attached to their corresponding electrical contact pads of the main board by a solder connection (7), for claim 8, the edge of the main board adjacent the mounting area includes a slot (51) with adjacent tab portions (see figure 2) to receive the second face of the connector board, for claim 9, the connector board comprises slots (see figures 5 and 6) for receiving the tab portions (33) of the main board, for claim 12, the connector board is a printed circuit board with traces that electrically connect the connecting pins.

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6. Claims 17 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Andrews, Jr. et al (4,715,820).

Andrews, Jr. et al discloses for claim 17, a first face and a second face and a thickness having slot (30) for receiving a main printed circuit board (22) and at least one through hole (38) between the first and second faces configured to receive a plurality of connector pin (18), for claim 18, at least some of the plurality of holes are aligned in two rows between which the slots for receiving a main printed circuit board are located (see figure 1).

## Claim Rejections - 35 USC § 103

- 7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 8. Claims 2, 5 and 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Hanni et al (4,109,298, cited in IDS) in view of Dola et al (4,762,500).

Hanni et al discloses all the limitations of claims 1, 3 and 4, as shown above,

-However, Hanni et-al-does not disclose:

a) The connector pin having a flange. Dola et al disclose a connector pin having a flange (26, see figure 3), therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention for Hanni et al to have the connector pin having a flange in view of Dola et al to stabilize the pin on the circuit board.

#### Contact

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Javaid Nasri whose telephone number is 571 272 2095. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynn Feild can be reached on 571 272 2800 ext 39. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any correspondence to this action may be mailed to:

Commissioner for Patents Post Office Box 1450 Alexandria, VA 22313-1450

For additional information regarding this new address, which was effective May 1, 2003, see

Correspondence with the United States Patent and Trademark Office, 68 Fed. Reg. 14332

(March 25, 2003).

**Or faxed to**: 703-308-7722 or 308-7724 (informal or draft communications should be clearly labeled "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to:

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Crystal Plaza 4, Fourth Floor (receptionist)

2201 South Clark Place, Arlington, Virginia

Javaid Nasri

Primary Examiner Art Unit 2839

JN jhn July 26, 2004